REMARKS

Claims 1-12 are currently pending in this application. The Examiner has rejected Claims 1-12 on various grounds as discussed below. By the present amendment, the Applicants have amended Claims 1, 5, 6, and 9. The Applicants respectfully traverse the rejections and request reconsideration of the claims as amended in view of the following remarks.

Claim 6 was rejected under 35 U.S.C. as being indefinite for failing to point out and distinctly claim the subject matter which the applicant regards as the invention. The Examiner asserts that it is unclear what the phrase "chip select signal" in Claim 6 may refer to. By the present amendment Claim 6 has been amended to refer to "the chip select signal" instead of to "a chip select signal". This change makes it clear that the chip select signal in Claim 6 is the same chip select signal referred to in Claim 5, from which Claim 6 depends.

The independent Claims 1, 5, 9 and 11 were rejected under 35 U.S.C. 102 as being anticipated by McClear et al. U.S. Patent 5,592,509. The Examiner has asserted that McClear: provides apparatus for preventing contention on a data bus; teaches control logic 174 having an input for receiving a CPU chip select signal and an output for providing a peripheral control signal which ends at a preselected time before the end of the read operation; the control logic being connected to a control input of the peripheral and to the output enable input of the transceiver; and a buffer connected to the address output of the cpu and an address input of the peripheral device, the buffer having an output enable input connected to the chip select signal. Applicants disagree with each of these characterizations of the McClear reference.

The primary teaching of McClear is that it provides a common bus transceiver which does not have control signal connections to a controlling CPU or to a peripheral. A stated advantage of the transceiver of McClear is that it has neither an output enable input or a direction input. The only place such inputs are mentioned in McClear is with reference to Fig. 1, which is described as prior art. McClear says that such inputs are a problem which is solved by the teachings of the McClear disclosure. Since the control logic 174 is part of the transceiver of McClear which does not have any control line connections to the CPU or a peripheral, it is not possible for the control logic 174 to

have an input for receiving a chip select signal from the CPU or an output for providing a peripheral control signal, and it is not possible for the control logic to be connected to a control input of the peripheral and to the output enable input of the transceiver.

The control unit 174 of McClear is a "collision arbitration" unit which prevents both output drivers 29 and 79 of the transceiver itself from operating at the same time. This does not prevent outputs of the cpu and the peripheral from driving signals onto the bus at the same time which is a problem solved by the present invention. At column 9, lines 40-50, McClear makes it clear that the transceiver itself does not avoid "bus clashing", which appears to correspond to contention. McClear states that:

> "...it is important that the system be one where it is known when data will be transmitted by the various devices, so that no bus clashing occurs. ... For example, in Fig. 5 microprocessor 81 might send out a read request to ASIC 85. Once the request is sent, the microprocessor knows data is expected back from the ASIC 85 device and therefore will not put data out on the bus until the read data is received."

This statement of McClear recognizes part of the problem solved by the present invention, but does not provide a solution. McClear implies that the CPU must wait until it has received the data. This solution has two problems. Waiting means that the system will be slowed, which is not desirable. It also suggests that once the data is "received" it would be safe for the CPU to "put data out on the bus", i.e. write or drive data onto the bus. But, as taught by the present inventors, just because the CPU has received, i.e. read, the data does not necessarily mean that the peripheral is no longer driving data onto the bus. There is a certain time lag between the end of the data select signal and the time at which the output of the peripheral actually goes to the high impedance state. The teachings of McClear do not solve these problems. But, the teachings of the present inventors do solve these problems.

In the present invention, transceivers corresponding to the Fig. 1, prior art, receivers of McClear are used in the common busses. These transceivers include an output enable input, designated G in McClear. In the present invention, control signals to the transceiver and the peripheral are changed before the end a designated read

time period. In the disclosed embodiment, these control signals are designated the data strobe signal for the peripheral and the output enable for the transceiver. After these signals are changed, the outputs of the peripheral and the transceiver transition to the high impedance state at least by the end of the read period. However, the transceiver has bus hold circuitry which maintains its last output level until a low impedance driver changes the level at the output. As a result, the cpu can read data at the proper time at the end of the read period. Since the peripheral and transceiver outputs are in the high impedance state when the cpu reads data, the cpu may immediately thereafter begin a write cycle and drive data onto the common bus without contention.

By the present amendment, independent Claims 1, 5, and 9 have been amended to explicitly claim in the first element that the transceiver has an output enable input, that is a control signal input. Each of these claims as originally written included the connection or coupling of a control signal to the output enable input of the transceiver. Independent Claim 11 included the output enable input as originally written in both the first element and in the last element. The presence of the control input for the transceiver clearly distinguishes the presently claimed invention from that of McClear, which does not have control connections from or to the cpu or the peripheral. As discussed above, the present invention provides a practical solution for a bus contention problem which to some extent was recognized by McClear, but for which McClear did not provide a solution.

In view of the above remarks the Applicants submit that the independent claims are patentable over the cited reference. Since the independent claims have been shown to be patentable over the cited reference, the Applicants submit that the dependent claims are also patentable over the cited reference. Allowance of Claims 1-12, as amended, is respectfully requested.

The Commissioner is hereby authorized to charge payment of any further fees associated with any of the foregoing papers submitted herewith, or to credit any overpayment thereof, to Deposit Account No. 21-0765, Sprint.

Applicants respectfully submit that the present application as amended is in condition for allowance. If the Examiner has any questions or comments or otherwise feels it would be helpful in expediting the application, he is encouraged to telephone the undersigned at (972) 731-2288.

Respectfully submitted,

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